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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,201	03/12/2004	Jeoung-Mo Koo	8021-205 (SS-17942-US)	7424

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,201	KOO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-8,16 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-26* is/are allowed.

6)☒ Claim(s) *1,2,6-8 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 24, 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 6-7 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Hutter et al. (US Pat. No. 5,576,233).

Regarding claim 1, Hutter et al. teaches a one-time programmable memory device, comprising:

an isolation layer (35) for defining an active area of a substrate (5) [see figs. 1 and 2g];

an oxide layer (38) formed on the active area [see fig. 2g];

a floating gate (19 or POLY-1) formed over the active area and the isolation layer (35) [see fig. 2g, specifically the cross section taken along the 2-2 line];

an inter-gate dielectric layer (50, 52) formed on the floating gate [see fig. 2g]; and

a control gate (25 or POLY-2) formed on the inter-gate dielectric layer [see fig. 2g], wherein a first portion of the floating gate (consider the portion of POLY-1 provided over gate dielectric 38 as shown in figures 1 and 2g, specifically the cross section taken along the 2-2 line) formed ever the active area is narrower than a second portion of the floating gate formed over the isolation layer (consider the portion of POLY-1 provided over isolation structure 35 as shown in figures 1 and 2g, specifically the cross section taken along the 2-2 line), and wherein the control gate (POLY-2) is formed over the second portion of the floating gate (POLY-1) and not over the first portion of the floating gate [see fig. 2g, specifically the cross section taken along the 2-2 line], and wherein an area of the isolation layer (Area 2) covered by the second portion is greater than an area of the isolation layer (Area 1) covered by the control gate [see fig 2g, below].

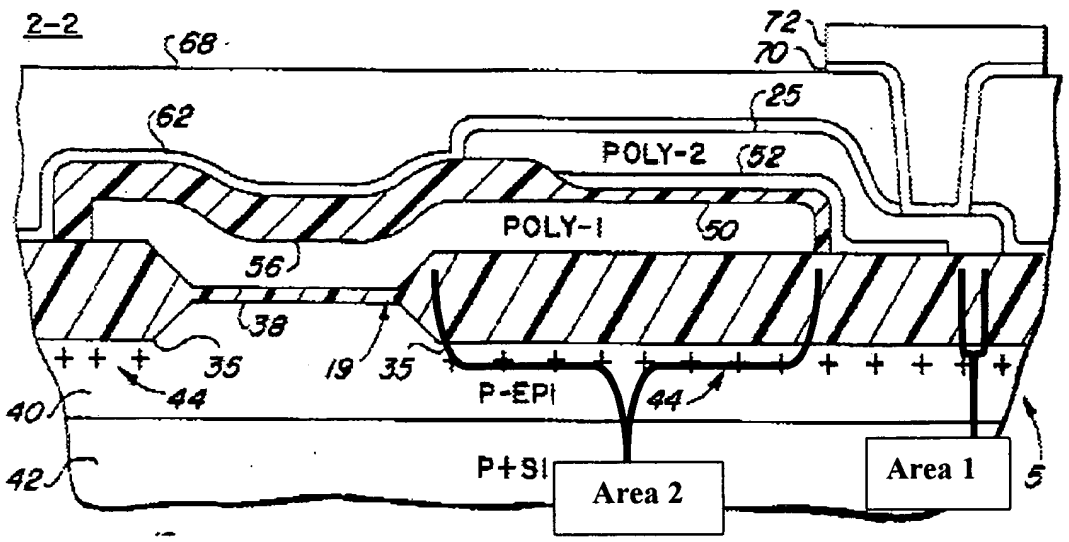

Fig. 2g

Regarding claim 2, Hutter et al. teaches a source region and a drain region (21, 27) formed in the active area at least one of under or adjacent both sides of the floating gate (POLY-I) [see fig. 2g, specifically the cross section taken along the 1-1 line].

Regarding claim 6, Hutter et al. teaches that the inter-gate dielectric layer includes a silicon nitride layer (52) [see col. 7, line 1].

Regarding claim 7, Hutter et al. teaches that the inter-gate dielectric layer includes a composites layer having a silicon oxide layer (50) and silicon nitride layer (52) [see col. 7, line 2].

Regarding claim 16, Hutter et al. teaches an integrated circuit, comprising:

a plurality of isolation layers (35) for defining a first area [see fig. 2g, cross section taken along line 2-2], a second area [see fig. 2g, cross section taken along line 1-1], and a third area [see fig. 2g, cross section taken along line 3-3] in a substrate (5);

a memory device [see cross section taken along line 2-2 in fig. 2g] including a floating gate (POLY-1) formed over the first area and at least one isolation layer (35) of the plurality of isolation layers, an inter-gate dielectric layer (50, 52) formed on the floating gate and including a composite layer having a silicon oxide layer (50) and a silicon nitride layer (52) [see col. 7, line 2], and a control gate (POLY-2) formed on the inter-gate dielectric layer [see cross section taken along line 2-2 in fig. 2g];

a first transistor [see NMOS transistor 15 taken along line 1-1 in fig. 2g] including a first gate (POLY-1) formed of the same material as the control gate (POLY-2), wherein the first gate (POLY-1) is formed in the second area of the substrate on a first gate oxide layer (consider layer 38 in fig. 2g, taken along line 1-1) having a thickness equal to a thickness of a tunnel oxide layer (consider layer 38 in fig. 2g, taken along line 1-1) formed on the substrate (5), and a first source region and a first drain region (21, 27) formed in the second area at least one of under or adjacent both sides of the first gate [see cross section taken along line 1-1 in fig. 2g]; and

a second transistor (see diode 11 taken along line 3-3) including a second gate (POLY-1) formed of the same material as the control gate (POLY-2), wherein the second gate (POLY-1) is formed in the third area of the substrate on a second gate oxide layer (14) thinner than the first gate oxide layer (38) [see fig. 2a, taken along lines 1-1 and 3-3], and a second source region and a second drain region (13) formed in the third area at least one of under or adjacent both sides of the second gate [please note that regions 13 are formed by the same ion implantation used to formed source/drain regions 21, 27. See col. 5, lines 38-41], wherein a first portion of the floating gate

(consider the portion of POLY-1 provided over gate dielectric 38 as shown in figures 1 and 2g, specifically the cross section taken along the 2-2 line) formed ever the active area is narrower than a second portion of the floating gate formed over the isolation layer (consider the portion of POLY-1 provided over isolation structure 35 as shown in figures 1 and 2g, specifically the cross section taken along the 2-2 line), and wherein the control gate (POLY-2) is formed over the second portion of the floating gate (POLY-1) and not over the first portion of the floating gate [see fig. 2g, specifically the cross section taken along the 2-2 line].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hutter et al. (US Pat. No. 5,576,233) in view of Bhattacharya et al. (US Pat. No. 6,339,000 B1).

Regarding claim 8, Hutter et al. fails to teach a three-layer inter-gate dielectric structure consisting of oxide, nitride and oxide. However, Bhattacharya et al. teaches that it is well known in the art to use a three-layer inter-gate dielectric structure consisting of oxide, nitride and oxide [col. 2, lines 14-20].

Hutter et al. and Bhattacharya et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would

have been obvious to a person of ordinary skill in the art to include a three-layer inter-gate dielectric structure consisting of oxide, nitride and oxide. The motivation for doing so, as is taught by Bhattacharya et al., is to enhance the charge retention capability of the floating gate (col. 2, lines 11-20). Therefore, it would have been obvious to combine Bhattacharya et al. with Hutter et al. to obtain the invention of claim 8.

Allowable Subject Matter

6. Claims 24-26 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a integrated circuit comprising a second gate oxide layer which is thinner than a tunnel oxide layer, and a first gate oxide layer which is thicker than the tunnel oxide layer and the second gate oxide layer as instantly claimed, and in combination with the additional limitations.

Response to Arguments

8. Applicant's arguments filed July 24, 2006 have been fully considered but they are not persuasive.

First, applicant argues that Hutter fails to teach the areas of the isolation layer as recited in claim 1. However, after a carefully review of the cited reference, it is believes that Hutter still teaches the argued limitations. For instance, fig 2g shows a view taken along 2-2 line in which an area of the isolation layer covered by the floating gate (area

2) is greater than the area covered by the control gate (area 1) [see rejection above]. Thus, Hutter clearly anticipates the claimed limitation.

In addition, applicant argues that Hutter fails to teach the limitation that the second gate oxide layer is thinner than the first gate oxide layer. However, it is noted that this limitation is taught by Hutter in column 6, lines 38-40 and 45-46. For instance, Hutter teaches a thermal oxide (14) having a thickness of 100 Å and a gate oxide (38) having a thickness of at least 200 Å. Thus, the thermal oxide (14) is thinner than the gate oxide (38) since a thickness of 100 Å is less than a thickness of 200 Å.

Therefore, for at least these reasons the rejections are considered to be proper.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727.. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KENNETH PARKER
SUPERVISORY PATENT EXAMINER

José R. Díaz
Examiner
Art Unit 2815